

FIG. 2A FIG. 2B FIG. 2C FIG. 2D FIG. 2E

FIG. 3

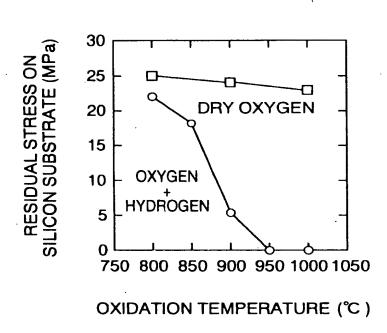


FIG. 4

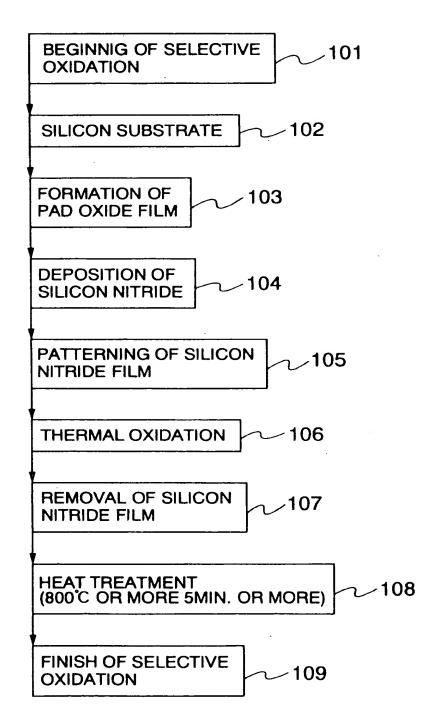


FIG. 5A

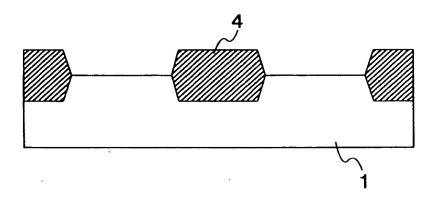
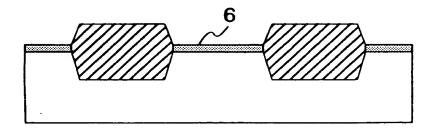


FIG. 5B



## FIG. 6

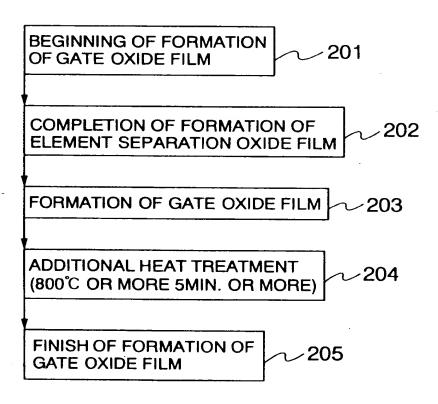


FIG. 7A

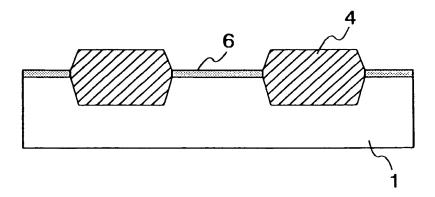


FIG. 7B

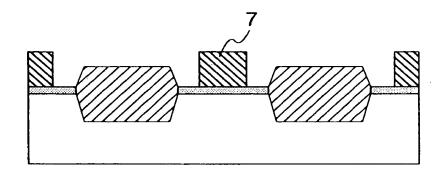
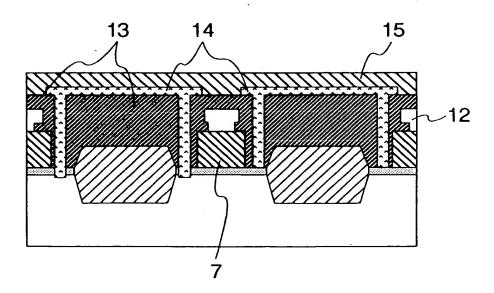
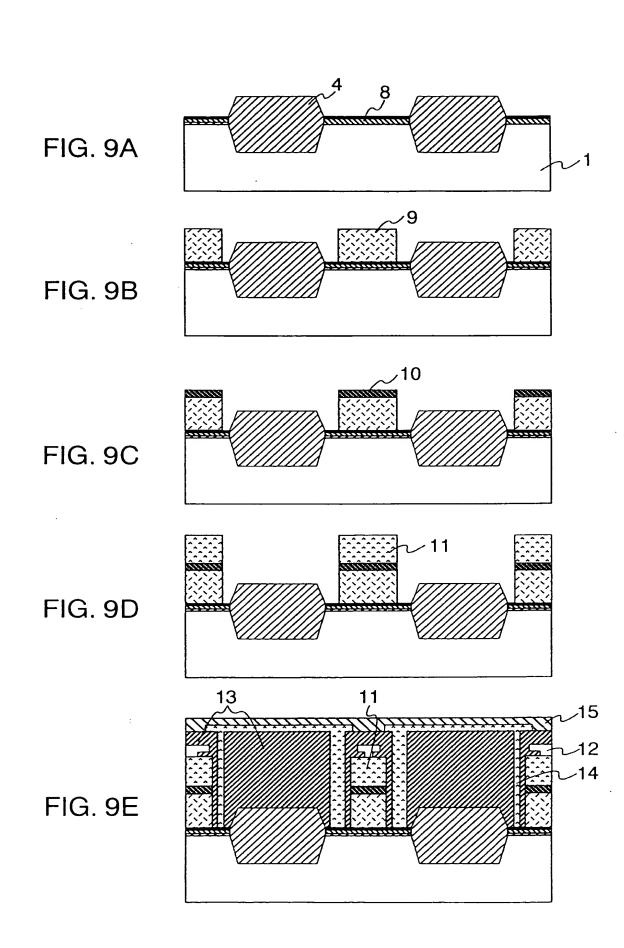


FIG. 7C



## FIG. 8

BEGINNING OF FORMATION OF TRANSISTOR STRUCTURE
COMPLETION OF FORMATION 302 OF GATE OXIDE FILM
DEPOSITION AND PROCESSING OF GATE ELECTRODE FILM 303
ADDITIONAL HEAT TREATMENT (800°C OR MORE 5MIN. OR MORE)
<u> </u>
FORMATION OF GATE ELECTRODE 305
INTRODUCTION OF IMPURITIES 306
FORMATION OF FIRST LAYER WIRING 307
FORMATION OF INTER LAMINAR 308
INSOLATING FILM
$\downarrow$
FOR MATION OF SECOND LAYER WIRING 309
<u> </u>
FORMATION OF INSULATING FILM 310
<u> </u>
COMPLETION OF FORMATION OF
TRANSISTOR STRUCTURE





## FIG. 10

